**Bangladesh University of Engineering and Technology**

**Department of Electrical and Electronic Engineering**

**EEE 303: Digital Electronics (July 2022)**

**Assignment 1 (Replaces Class Test 2)**

**Time:** 20 min **Due** **Date:** 01 Feb 2023 **Total Marks:** 20 **Term**: July 2022

**Student ID**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1 | 8 | 0 | 6 | x | y | z |

**Student Name:**

**Student Name**

***Your code solutions should be your own work. Partial marks may be given for incomplete efforts, however, plagiarized or copied solutions will result in ZERO in this assignment.***

***This file is to be used as a template for submitting your solution.***

**Q1. Calculate the Parameters X, Y, T. Write your answers in your script. These parameters are to be used in Q2 and Q3**

**X = 32 bit number with your student ID in BCD**

**(eg if your student ID is 1706001, X=01706001|16 = 24141825|10)**

**Y = 8 bit number, with each byte of X (eg if your student ID is 1706001, Y=(01+70+60+01)|16 = D2|16)**

**T = ((X\*3+5) mod 16) (eg if your student ID is 1706001, T = 8)**

**Ans:**

**X =**

**Y =**

**T =**

**Q2. A Verilog function has input [4:0]A, Clk, I and S, and output [7:0]B. The system has a memory [3:0]M. If S=0, the output will be in high-impedance state, regardless of the state of the Clk. If S is changed from 1 to 0, output will be immediately high-impedance state (S is Asynchronous, or Clk independent).**

**If S=1, the output will change only at the positive edge of Clk (0 to 1 transition):**

**If I=1, the M will be initialized to 4’b0000 (M must be initialized by your test bench). B will be 8’x0**

**If I =0, then M and B will be updated in the following manner:**

**If (M=0): B will be the lowest (0th) byte of X (eg. 01 of the 01706001)**

**If (M=1): B will be the 1st byte of X (eg. 60 of the 01706001)**

**If (M=2): B will be the 2nd byte of X (eg. 70 of the 01706001)**

**If (M=3): B will be the upper (3rd) byte of X (eg. 01 of the 01706001)**

**If (M>3 and M < 16): B = Fibb(M-2) + Y + A**

**M will be incremented by 1**

**Ans:**

**Explain your logic how you will solve the problem:**

**Verilog Code:**

**// Your Verilog code goes here for the module.**

**Q3. Design an appropriate test bench in SystemVerilog to test the module in Q2.**

**Your test bench should show output for the function for representative test cases of the input, with time-step of T between each successive steps. Show waveform for your solution. Waveform should include both binary and Hexadecimal value of the required variables, and should be clearly legible in a printout. Use EDAPlayground for this part.**

**Verilog Code:**

**// Your testbench code goes here for the module.**

**Output:**

**// Paste the output here**

**Paste wave forms from GTKWave here**

**Q4. Modify the testbench in Q3, so that the Verilog module is given the digits of X sequentially in each clock pulse in a repetitive manner.**

**Verilog Code:**

**// Your testbench code goes here for the module.**

**Output:**

**// Paste the output here**

**Paste wave forms from GTKWave here**

**Q5. Prepare a short video presentation where you explain your solution and demonstrate the code execution. Use Zoom with screen sharing to record your video. Keep the recording under 5 minutes. Paste a link to the video (Microsoft Stream Link preferred, OneDrive/Google Drive/YouTube is also acceptable. The video should be “unlisted” or not publicly searchable in all cases, with link sharing open to public. The video should be available for view until the result is published for this semester).**

**Write the link to your video below:**

**Ans:**

https://